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Benchmarking of Straddle-Gate MOSFETs

ABSTRACT

The performance of a promising non-classical MOSFET concept called straddle-gate FET is investigated by device simulation. The off-currents, on-currents, and intrinsic gate delay times of straddle-gate FETs with gate lengths in the 37-9nm range are calculated and compared to the performance of conventional sidewall-spacer MOSFETs. It is shown that straddle-gate FETs deliver considerably higher on-currents compared to spacer MOSFETs at comparable off-current levels. Non-optimized straddle-gate transistors meet the ITRS on- and off-current targets for high-performance logic transistors at the 37, 25, and 18nm gate length levels.

1. INTRODUCTION

Continuous MOSFET scaling according to Moore's Law has been the driver in Si VLSI electronics during the last decades. To continue this trend successfully in the future, the 2003 edition of the ITRS requires production stage MOSFETs with gate lengths of 18nm in the year 2010 and 9nm in the year 2016 (for high-performance logic) [1]. Experimental transistors with such short gates showing typical MOSFET switching behavior have already been realized in different labs, see, e.g. [2-4]. However, these devices suffer from short channel effects and do not meet the ITRS performance targets, such as the on-current I_{on} and the off-current I_{off}. High on-current and sufficiently low off-current are needed simultaneously to achieve small gate delays, i.e., high switching frequencies, and low standby powers.

Several non-classical MOSFET concepts, such as transport enhanced FETs (e.g., strained Si FETs), vertical and planar double-gate MOSFETs, and tri-gate MOSFETs, are intensively investigated to improve the electrical performance of extremely scaled transistors. Two recent studies revealed, however, that so far neither classical nor non-classical MOSFETs with gate lengths below 30nm could be realized that simultaneously meet the I_{on} and I_{off} targets [5-6]. Instead, the gap between the required and

experimentally obtained performance widens considerably in the sub-25nm gate length range. Figure 1 shows the on-currents of recently published nanometer MOSFETs as a function of gate length together with the ITRS on-current targets (for high-performance logic transistors) [6]. The on-currents have been extracted from reported MOSFET output and transfer characteristics under the constraint that the ITRS off-current target is hit and that the supply voltage conditions specified in the ITRS are fulfilled. It can be seen that currently the best reported MOSFETs deliver less than 50% of the required on-current at the 14nm gate length level and less than 20% for 10nm gate length [6]. The dramatic trend shown in [6] makes clear that the scaling potential and the ability to meet the ITRS performance targets of every possible MOSFET concept should be carefully assessed.

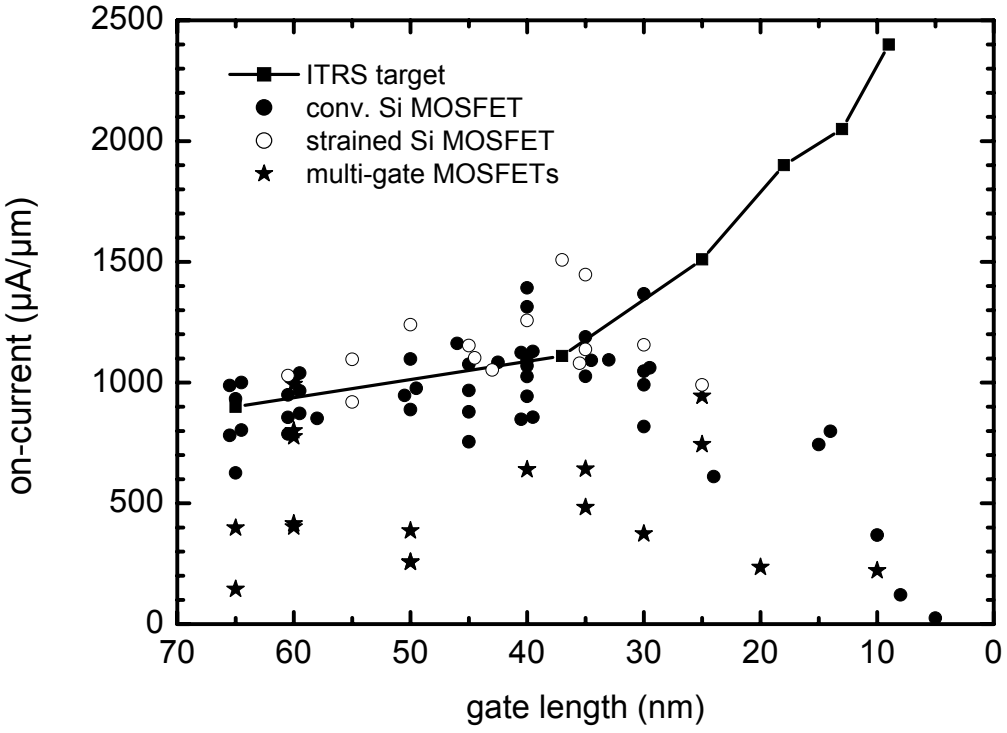

Figure 1- Extracted on-currents of reported nanometer MOSFETs [6].

The aim of the present work is to estimate the potential of a non-classical MOSFET concept called fully depleted SOI straddle-gate transistor by device simulation and to compare its performance with that of conventional sidewall-spacer SOI MOSFETs. In Sec. 2 the straddle-gate concept is introduced and in Sec. 3 we discuss the simulated transistor structures. Section 4 presents the result of our study and Sec. 5 concludes the paper.

2. THE STRADDLE-GATE CONCEPT

The straddle-gate concept is not really new and has been introduced more than 10 years ago [7-8]. Compared to other non-classical MOSFET designs, however, it has attracted less attention so far. The basic idea is to separate the doped source and drain extensions from the active channel of the MOSFET by a gated low threshold voltage region. The cross section of a possible straddle-gate MOSFET design is shown in Fig. 2a. It is an SOI structure consisting of two gate contacts, and highly doped (n^+) elevated source/drain regions separated by a lightly doped p-type channel layer. The inner gate (above the center of the channel layer) switches the transistor on or off and corresponds to the gate of a conventional MOSFET. The conductivity of the channel region between the source/drain regions and the inner gate is controlled by a second gate called the outer gate. The same potential is applied to the outer and inner gates, i.e., $V_{Go}=V_{Gi}=V_G$. The condition for proper straddle-gate FET operation is that the threshold voltage of the outer MOS structures (outer gate / oxide / channel layer), V_{tho}, is lower than the threshold voltage of the inner transistor (inner gate / oxide / channel layer), V_{thi}. This condition can easily be fulfilled by using different gate materials, where the work function of the outer gate, Φ_o, is lower than the work function of the inner gate, Φ_i (see Fig. 3a).

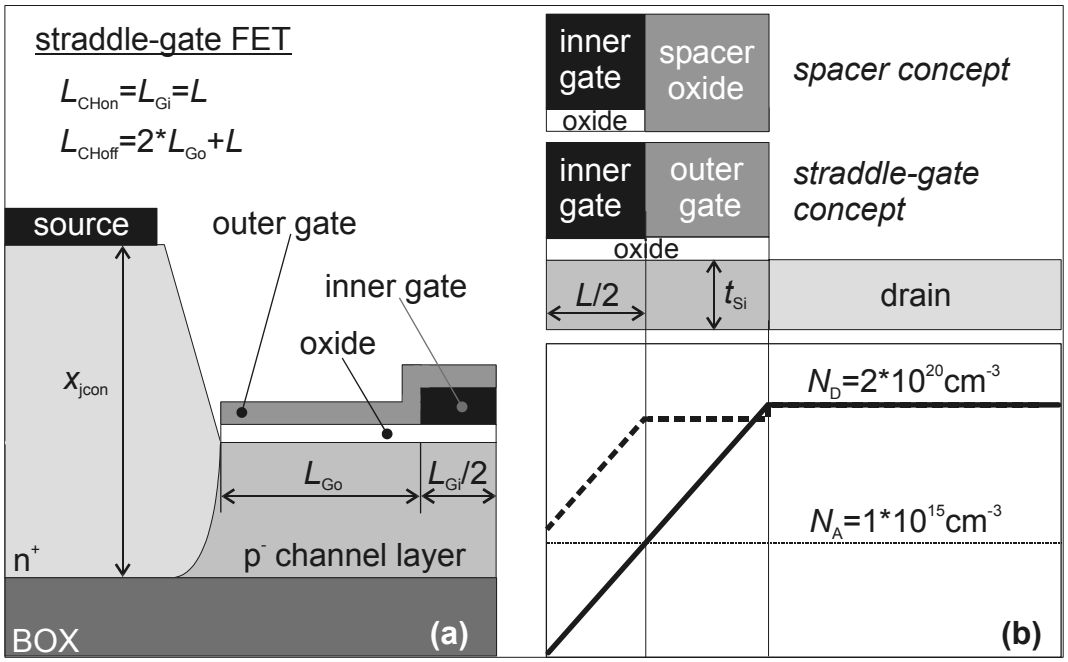

Figure 2- (a) Cross section and (b) lateral doping profile of the straddle-gate (full line) and spacer FETs (dashed line).

For zero gate voltage, the inner and outer transistors are switched off. If the gate voltage becomes more positive, an electron inversion layer is formed underneath the outer gate and the outer transistor becomes switched on at $V_G = V_{tho}$, while the inner transistor is still switched off. Finally, once V_G exceeds V_{thi}, the inner transistor is switched on as well and a drain current can flow. Thus, the channel length of the straddle-gate FET varies with V_G. In the on-state ($V_G > V_{thi}$, i.e., inner and outer transistor switched on) the channel length of the transistor, L_{CHon}, is equal to the length on the inner gate, L_{Gi}. In the off-state ($V_G = 0$), however, the channel length is $2 \times L_{Go} + L_{Gi}$.

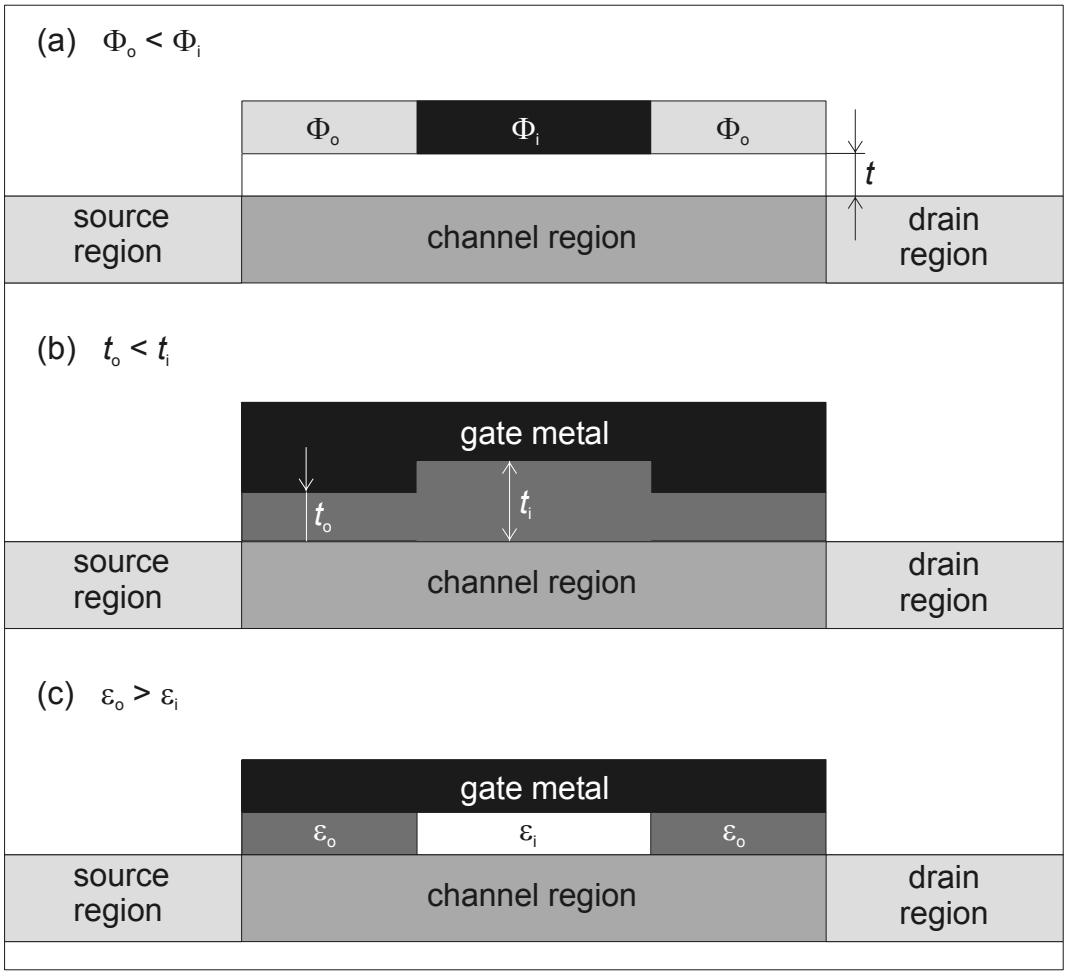

Figure 3- Cross section of different design variations of straddle-gate FETs. (a) Straddle-gate transistor with different gate materials for the inner and outer gates. (b) Straddle-gate transistor with different thicknesses of the gate dielectric in the inner and outer gate stacks. (c) Straddle-gate transistor with different inner and outer gate dielectrics.

In principle, there are further options to fulfill the condition $V_{tho} < V_{thi}$, e.g., by

- using a thinner gate dielectric in the outer transistor compared to the inner transistor (see Fig. 3b),
- using different outer and inner gate dielectrics (see Fig. 3c).

3. SIMULATED STRUCTURES

The cross section of the straddle-gate FETs investigated in this work is shown in Fig. 2. Transistors with inner gate lengths $L_{Gi}=L$ of 37nm, 25nm, 18nm, and 9nm have been simulated. The lateral abruptness of the source/drain doping, *LA*, the equivalent oxide thickness, *EOT*, the thickness of the elevated source/drain, x_{jcon}, and the supply voltage V_{DD} have been chosen according to the 2003 edition of the ITRS (see Tab. 1).

technology node	*L* nm	*EOT* nm	*LA* nm/dec	x_{jcon} nm	L_{Go} nm	V_{DD} V	I_{off} µA/µm	I_{on} µA/µm
hp90	37	1.2	4.1	40.7	21.7	1.2	0.05	1110
hp65	25	0.9	2.8	27.5	14.8	1.1	0.07	1510
hp45	18	0.7	2.1	19.0	11.1	1.0	0.10	1900
hp22	9	0.5	1.3	10.0	6.9	0.8	0.50	2400
$N_{SD}=N_D=2.0\times10^{20}cm^{-3}$, $N_{CH}=N_A=1.0\times10^{15}cm^{-3}$, t_{Si}=5nm								

***Table 1*-** Transistor design parameters and ITRS targets for high-performance logic transistors.

The outer gate is made of n^+ polysilicon (Φ_o=4.14eV) and different values for Φ_i have been assumed. For comparison, conventional SOI spacer FETs have been simulated as well. Their design is identical to that of the straddle-gate FETs apart from the two following exceptions:

- the outer gate is replaced by SiO_2 sidewall spacers,
- the doping of the channel layer underneath the spacers is assumed to be higher ($N_D=10^{19}cm^{-3}$) to guarantee fairly low series resistances.

The doping profiles and design details of the straddle-gate FETs and the conventional spacer FETs are shown in Fig. 2b. Table 1 summarizes the dimensions of the investigated FETs and the ITRS targets for the supply voltage, and the off- and on-currents. For the simulations, the commercial device simulator ATLAS / S-PISCES has been used. To take nonstationary transport effects into account, a modified drift-diffusion

model similar to that developed in [9] has been implemented in the simulator. It has been shown that this model results in velocity profiles in the channels of extremely scaled single- and double-gate MOSFETs very close to those predicted by Monte Carlo simulations.

4. RESULTS AND DISCUSSION

The dc characteristics of n-channel straddle-gate and sidewall spacer FETs with the designs described in Sec. 3 have been simulated. In the following, we concentrate on the on- and off-currents. The on-current, I_{on}, is the drain current I_D for the case that both the gate voltage V_G and the drain voltage V_D are equal to the supply voltage V_{DD} specified in the ITRS (see Tab. 1), and the off-current, I_{off}, is I_D for $V_G = 0$ and $V_D = V_{DD}$. Note that V_{DD} is required to decrease for decreasing gate length while the on-currents should increase. Figure 4 shows the I_{on} vs. I_{off} characteristics of straddle-gate and spacer FETs with gate lengths of 37nm, 25nm, and 18nm. Straddle-gate FETs with different work functions of the inner gate of 4.71 (midgap, on the left), 4.60, 4.50, 4.40, 4.33 (titanium), and 4.28eV (on the right) have been simulated. For the spacer FETs, we use the same values for the gate work function. Additionally, spacer FETs with an n^+ polysilicon gate ($\Phi = 4.14$ eV, very right in Fig. 4) are considered. The general trend is the same for all simulated transistors: a decreasing gate workfunction leads to a smaller V_{th} and thus to higher on- and off-currents. The most important result is that the on-currents of the straddle-gate FETs with L=37nm, 25nm, and 18nm are considerably higher than those of spacer FETs (at comparable I_{off} levels).

Taking the FETs with a gate workfunction of 4.60eV as an example, the following I_{on} / I_{off} ratios (I_{on} and I_{off} given in μA/μm) can be extracted from Fig. 4.

- Straddle-gate MOSFET: 1740/1.2×10^{-3} (37nm), 2070/7.4×10^{-3} (25nm), 2190/5.6×10^{-2} (18nm). The I_{on}-I_{off} data points are within the shaded area, i.e., the ITRS I_{on}-I_{off} targets are met.
- Spacer MOSFET: 1000/3.6×10^{-3} (37nm),1240/2.1×10^{-2} (25nm), 1380/0.15 (18nm). The I_{on}-I_{off} data points are close to, but outside the shaded area, i.e., the ITRS I_{on}-I_{off} targets are not met.

The simulated results for the spacer FETs qualitatively correspond to the performance of experimental FETs shown in Fig. 1. In the gate length range between 30 and 37nm only the very best conventional FETs scarcely meet the I_{on} target. Only strained Si MOSFETs in this gate lengths range show on-currents clearly above the ITRS target.

For a channel length of 9nm neither the straddle-gate nor the spacer FETs simulated in

this study meet the ITRS targets. The straddle-gate FETs still show considerably higher on-currents at comparable I_{off}-levels. Furthermore, 9nm straddle-gate FETs having Φ_i=4.40eV and below meet the ITRS I_{on} target of 2400µA/µm, but show to high off-currents.

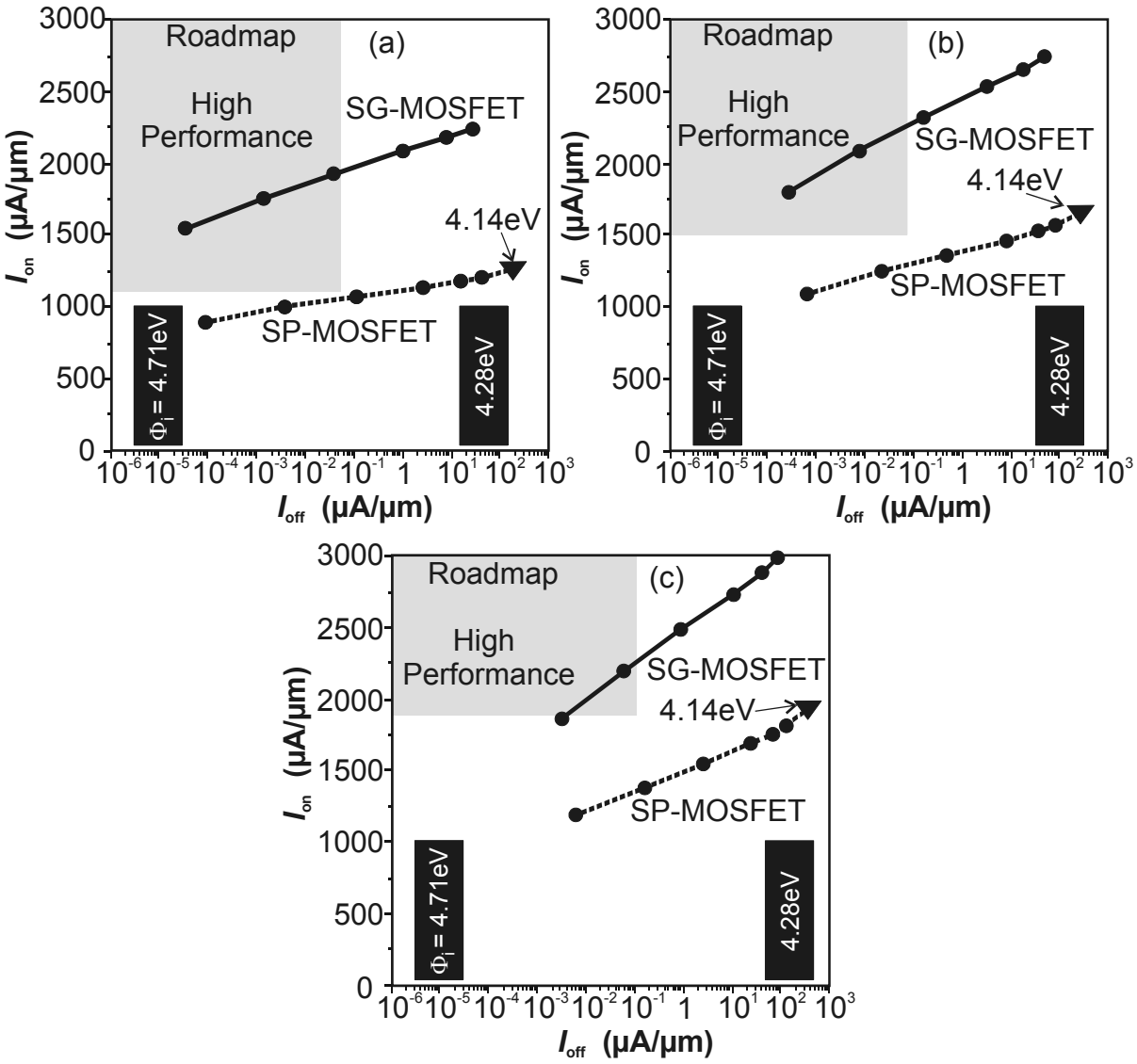

Figure 4- I_{on} vs. I_{off} for straddle-gate and spacer FETs with (a) L=37nm, (b) 25nm, and (c) 18nm. The shaded areas mark the ITRS I_{on}-I_{off} targets. Transistors, whose I_{on}-I_{off} data points are within the shaded areas, meet the ITRS targets.

The results of our studies indicate that straddle-gate FETs have a clear edge over spacer FETs concerning the I_{on}-I_{off} performance (see Fig. 4). The main reason is the channel length variation in straddle-gate FETs when switching the transistor from off to on. In the on-state, the straddle-gate FET behaves like a short channel transistor (high on-current) and in the off-state like a transistor with a longer channel (low off-current).

To make a fair comparison between straddle-gate and spacer FETs, not only the current, but also the gate capacitance C_G and the intrinsic delay time τ should be considered. Due to the larger total gate length $L=2\times L_{Go}+L_{Gi}$, straddle-gate FETs have much larger gate capacitance compared to spacer FETs. Thus, the intrinsic delay time (defined as $\tau = C_G \times V_{DD} / I_{on}$) of the straddle-gate FET will be higher compared to the spacer FET as well.

Table 2 compares the calculated τ of straddle-gate and spacer FETs that just fulfill the ITRS I_{off} target. To obtain the required off-current, the gate workfunctions of the transistors have been adjusted. The gate capacitance used to calculate the intrinsic delay time is the oxide capacitance (normalized to the gate width) calculated by $C_G=\varepsilon_{SiO2}\times L / EOT$ [1].

technology node	design	Φ_i eV	τ_{sim} ps	τ_{ITRS} ps
hp90	straddle	4.49	1.43	0.95
	spacer	4.53	1.21	
hp65	straddle	4.53	1.03	0.64
	spacer	4.56	0.82	
hp45	straddle	4.58	0.88	0.39
	spacer	4.61	0.66	

Table 2- Intrinsic delay time τ for straddle-gate and spacer FETs meeting the ITRS I_{off} target.

For all gate lengths, the straddle-gate FETs show slightly higher intrinsic delay times compared to the spacer FETs. This means that the higher on-current of the straddle-gate FET can only partially compensate the higher gate capacitance. However, it is important to note that in logic circuits, during switching not only the intrinsic capacitances of the transistors have to be charged or recharged. Instead, all parasitic capacitances of the circuit including fringing and overlap capacitances of the transistors as well as the capacitances of the interconnects have to be considered. Thus, when comparing the performance of straddle-gate and spacer FETs, the drawback of slightly higher intrinsic delay times of straddle-gate FETs should be less important for the overall circuit speed than the advantage of the much higher on-currents.

The performance of straddle-gate FETs can be further improved by design optimization. Possible options to improve the I_{on}-I_{off} -τ performance are

- optimization of the length of the outer gate L_{Go},
- optimization of the lateral doping profile of the channel layer and of the n^+ source and drain regions,
- introducing straddle-gate double-gate structures (e.g., for the 9nm gate length level).

It should be noted, that at least theoretically the performance of spacer FETs can also be improved. Let us take for example the 25nm spacer MOSFET design as described above, keep the n-type doping at the gate edges of $10^{19}cm^{-3}$, and let the doping increase towards source and drain regions with the doping gradient *LA* given in Table 1. Then the on-current increases by a factor of around 2 and the off-current, depending on the gate workfunction, by a factor of 2…12. For a gate workfunction of 4.71eV (midgap), the 25nm spacer FET will shown an I_{off} of 0.0003µA/µm and an I_{on} of 1665µA/µm, thus fulfilling the ITRS targets. This design requires, however, a spacer length of only around 3nm for the 25nm transistor. If the doping at the gate edge is increased to $5\times10^{19}cm^{-3}$ the spacer length of the 25nm FET will even smaller (around 1.5nm). Currently, it is impossible to fabricate such tiny spacers.

5. CONCLUSIONS

The performance of SOI straddle-gate and conventional sidewall-spacer FETs with gate lengths between 37nm and 9nm has been investigated by device simulation. The straddle-gate FETs show systematically higher on-currents compared to spacer FETs at comparable off-current levels. The I_{on} and I_{off} targets of the 2003 ITRS edition for high-performance logic transistors are met by the simulated non-optimized straddle-gate FETs (except for 9nm gate length). The larger gate capacitance of the straddle-gate structure leads, however, to slightly higher intrinsic transistor delay times. There are several options to optimize the design of the straddle-gate FETs and to further improve their performance. The present study shows that the straddle-gate FET is a promising option to meet the performance targets even at the end of the roadmap and should be further investigated.

6. ACKNOWLEDGEMENT

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